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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: David G. Figueroa et al.
Patent No.: 7,358,607
Issue Date: April 15, 2008

Examiner: Im, Junghwa
Group Art Unit: 2811
Docket No: 884.B23US1

Title: SUBSTRATES AND SYSTEMS TO MINIMIZE SIGNAL PATH DISCONTINUITIES (As Amended)

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Richard Beck
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Richard Beck
Signature

IN UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.:	7,358,607	Docket No:	884.B23US1
Issue Date:	April 15, 2008	Patentee:	David G. Figueroa et al.
Customer No.:	21186	Confirmation No.:	5260
Title	SUBSTRATES AND SYSTEMS TO MINIMIZE SIGNAL PATH DISCONTINUITIES (As Amended)		

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
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It is requested that a Certificate of Correction be issued correcting printing errors appearing in the above-identified United States patent. A copy of the text of the Certificate in the suggested form are enclosed.

Issuance of the Certificate of Correction would neither expand nor contract the scope of the claims as properly allowed, and re-examination is not required.

As the error is that of the Patent Office, it is believed that no fee is due.

The Examiner is authorized to charge any additional fees or credit overpayment to Deposit Account No.19-0743.

Respectfully Submitted,

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Date: May 13, 2008

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Name

Richard Beck
Signature

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,358,607

DATED : April 15, 2008

INVENTOR(S) : Figueroa et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 8, line 56, in Claim 4, delete "terminal;" and insert - - terminal of the die; - -, therefor.

In column 9, line 17, in Claim 8, after "plurality of" insert - - the - -.

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Atty Docket No: 884.B23US1

PATENT NO. _____7,358,607_____

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Note: **P** = USPTO Error **S** = SLWip Error
File#: **884.B23US1**
Proofread By: **Divyapreet (04/22/2008)**

US Serial No.: **10/090,735** US Patent No.: **US 7,358,607 B2** Issue Date: **Apr. 15, 2008**

Title: **SUBSTRATES AND SYSTEMS TO MINIMIZE SIGNAL PATH DISCONTINUITIES**

PR Instructions: **Face Page, Claims and Abstract**

Sr. No.	P/S	Original		Issued Patent		Description of Error
		Page	Line	Column	Line	
1	P	Page 3 Claims (10/29/2007)	Claim 8 Line 14	8	56	In Claim 4, delete "terminal;" and insert - - terminal of the die; - -, therefor.
2	P	Page 4 Claims (10/29/2007)	Claim 31 Line 8	9	17	In Claim 8, after "plurality of" insert - - the - -.

units). Embodiments of the present invention may be useable to construct the high performance links, switches, switch elements, channel adapters, etc., requiring high signal path integrity to satisfy NGIO or any other future technology's stringent requirements. One example would be an NGIO host channel adapter (HCA) chip or chipset package constructed utilizing an embodiment of the present invention to provide layered wiring though a layered substrate, with a resultant electrical conduction path having substantial impedance continuity maintained within a predefined limit therealong. Information with respect to NGIO can be found within the "*Next Generation Input/Output (NGIO) Specification*" as set forth by the NGIO Forum on Jul. 20, 1999, and also the "*Next Generation I/O Link Architecture Specification: HCA Specification, Revision* 1.0" as set forth by NGIO Forum on May 13, 1999.

In concluding, reference in the specification to one embodiment, an embodiment, an example embodiment, etc., means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of such phrases in various places in the specification are not necessarily all referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with any embodiment, it is submitted that it is within the purview of one skilled in the art to effect such feature, structure, or characteristic in connection with other ones of the embodiments. Furthermore, for ease of understanding, certain method procedures may have been delineated as separate procedures; however, these separately delineated procedures should not be construed as necessarily order dependent in their performance, i.e., some procedures may be able to be performed in an alternative ordering, simultaneously, etc.

This concludes the description of the example embodiments. Although the present invention has been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that may fall within the spirit and scope of the principles of this invention. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims, without departing from the spirit of the invention. In addition to variations and modifications in the component parts and/or arrangements, alternative uses may also be apparent to those skilled in the art.

For example, practice of the present invention is not limited to the above-mentioned reduction in capacitance, and a non-exhaustive listing of other benefits of deletion of build-up layers may be a decrease in signal path resistance or an number of inter-layer joints. With regard to the substrate arrangement, the practice of the present invention is not limited to the other FIG. **5** example layering arrangement, but instead, other arrangements may likewise be provided. For example, build-up layers may be eliminated on both sides of the core. In addition, the continuity of the signal may be improved, for example, by a non-exhaustive listing of: modification of dielectric permittivity of non-conductive layers so capacitance is reduced without physical modification of number of layers. Accordingly, any one or more of: reducing a number of layers; increasing a separation distance between impedance-interacting (e.g., capacitive) layers; and, a strengthening of dielectric permittivity of material disposed between impedance interacting layers, may be used anywhere along an electrical conducting path of a layering arrangement, so as to keep an impedance (Z) variation from neighboring point to neighboring point along the path, to below a predetermined value or percentage (e.g., 0 to 10 Ohms, 15 Ohms, or 0 to 10%, 15%, 20% etc.).

What is claimed is:

1. A substrate to mount a die having at least one input signal terminal, the substrate keeping an impedance variation between an input signal entering the substrate from a receiving substrate and an output signal provided to the at least one input terminal below a predetermined value, the substrate comprising:

a dielectric core member having an approximate thickness of 800 microns;

a first plurality of dielectric lamination layers on a first side of the dielectric core member, each having an approximate thickness of 30 microns, and wherein the dielectric core member comprises material of different dielectric permittivity in comparison to a permittivity of material of the dielectric lamination layers;

a second plurality of conductive layers on the first side of the dielectric core member, each having an approximate thickness of 25 microns, and including at least one connector on a first surface of an uppermost one of the second plurality of conductive layers to couple to the at least one input signal terminal of the die; and

a single conductive layer on a second side of the dielectric core member, having an approximate thickness of 17 microns, wherein the single conductive layer comprises at least one land to couple to the input signal from the receiving substrate.

2. The substrate as claimed in claim **1**, wherein the receiving substrate comprises one of an interposer or a motherboard.

3. The substrate as claimed in claim **1**, wherein the predetermined value is within the range of ±10 ohms.

4. A system comprising:

a die having a plurality of terminals, including at least one input signal terminal;

a receiving substrate having a plurality of terminals, including at least one terminal to provide an input signal;

a layered substrate including

a dielectric core member;

a first plurality of dielectric lamination layers on a first side of the dielectric core member, wherein the dielectric core member comprises material of different dielectric permittivity in comparison to a permittivity of material of the first plurality of the dielectric lamination layers;

a second plurality of conductive layers on the first side of the dielectric core member, including at least one connector on a first surface of an uppermost one of the second plurality of conductive layers, the connector being coupled to the at least one input signal terminal; and

a single conductive layer on a second side of the dielectric core member, wherein the single conductive layer comprises at least one land coupled to the input signal from the receiving substrate.

5. The system as claimed in claim **4**, wherein the receiving substrate comprises one of an interposer or a motherboard.

6. The system as claimed in claim **4**, wherein the predetermined value is within the range of ±10 ohms.

7. The system as claimed in claim **4**, wherein the dielectric core member has an approximate thickness of 800 microns, wherein each of the first plurality of dielectric lamination

layers has an approximate thickness of 30 microns, wherein each of the second plurality of conductive layers has an approximate thickness of 25 microns, and wherein the single conductive layer has an approximate thickness of 17 microns.

8. A substrate to mount a die having at least one input signal terminal, the substrate keeping an impedance variation between an input signal entering the substrate from a receiving substrate and an output signal provided to the at least one input terminal below a predetermined value, the substrate comprising:

a dielectric core member;

a first plurality of dielectric lamination layers on a first side of the dielectric core member, wherein the dielectric core member comprises material of different dielectric permittivity in comparison to a permittivity of material of the first plurality of dielectric lamination layers;

a second plurality of conductive layers on the first side of the dielectric core member, including at least one connector on a first surface of an uppermost one of the second plurality of conductive layers to couple to the at least one input signal terminal of the die; and

a single conductive layer on a second side of the dielectric core member, wherein the single conductive layer comprises at least one land to couple to the input signal from the receiving substrate.

9. The substrate as claimed in claim **8**, wherein the receiving substrate comprises one of an interposer or a motherboard.

10. The substrate as claimed in claim **9**, wherein the predetermined value is within the range of ±10 ohms.

11. The substrate as claimed in claim **10**, wherein the dielectric core member has an approximate thickness of 800 microns, wherein each of the first plurality of dielectric lamination layers has an approximate thickness of 30 microns, wherein each of the second plurality of conductive layers has an approximate thickness of 25 microns, and wherein the single conductive layer has an approximate thickness of 17 microns.

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